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A 2-D ANALYTICAL THRESHOLD VOLTAGE MODEL FOR SYMMETRIC DOUBLE GATE MOSFET'S USING GREEN'S FUNCTION

Anoop Garg*, S.N. Sinha, R.P. Agarwal

Indian Institute of Technology Roorkee,
Roorkee, 247667, Roorkee, India
* E-mail: ashugarg.iit@gmail.com

We propose a new two dimensional (2D) analytical solution of Threshold Voltage for undoped (or lightly doped) Double Gate MOSFETs. We have used Green's function technique to solve the 2D Poisson equation, and derived the threshold voltage model using minimum surface potential concept. This model is assumed uniform doping profile in Si *region. The proposed model compared with existing literature and experimental data and we obtain excellent agreements with previous techniques.*

Keywords: *GREEN'S FUNCTION, MINIMUM SURFACE POTENTIAL, THRESHOLD VOLTAGE, SYMMETRIC DG-MOSFET, TWO DIMENSIONAL (2D) POISSON EQUATIONS AND UNDOPED OR LIGHTLY DOPED.*

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NOMENCLATURE

$\in_{Si}$ $(\in_{ox})$	The dielectric permittivity of Si(SiO_2)
Q	The electronic charge
$\rho(x,y)$	The two-dimensional charge density
t_{ox}	The thickness of front and back gate oxide
t_{Si}	The thickness of Si film
n_i	The intrinsic carrier concentration of Si film
$L(W)$	The effective channel length (width)
C_{ox}	The capacitance per unit area of the front (back) gate oxide
C_{Si}	The capacitance per unit area of the Silicon film
V_{gs}	The gate-source voltage
V_{ds}	The drain-source voltage
V_{fb}	The flat band voltage of the front (back) gate
$K_n = {}^{n\Pi}/_{L}$	The Eigen value for x direction
$K_m = {}^{m\Pi}/_{t_{si}}$	The Eigen value for y direction
$D_{sf}(x)(D_{sb}(x))$	The electric displacement at the front (back) Si-Sio2 interface
$\Phi(x,y)$	The 2D potential distribution in Si region

$E_y(x,y)$	The 2D vertical electric field distribution in Si region
$\Phi_{f,inv}$	Surface potential at strong inversion condition
$\Phi_{f,inv} = 2\Phi_f$	
$\Phi_f = V_t \ln\left(\frac{N_A}{n_i}\right)$	
$\rho(x,y) = -qN_A f(y)$	
$x_{\min}$	Location of the minimum surface potential at the si surface
V_{th}	Threshold Voltage
ΔV_{th}	Threshold Voltage roll-off

1. INTRODUCTION

Bulk cmos has been the mainstream very large-scale integration (VLSI) technology for the past two decades. Double-gate (DG) MOSFET is becoming a subject of intense VLSI research because, in principle, DG-MOSFET's can be scaled to the shortest channel length possible for a given gate oxide thickness [1] the advantages of dg mosfets include: ideal 60 mv / dec sub threshold slope, scaling by silicon film thickness without high doping, setting of threshold voltage by gate work functions [4] etc. The key factors that limit how far a dg mosfet can be scaled come from short-channel effects (SCEs) such as threshold voltage roll off and drain induced barrier lowering (dibl) [6-7].

The analytical modeling of double gate MOSFET's has been reported by several authors [1-11]. Chen [8] has indicate of short channel effect, threshold voltage (V_{th}) roll-off has investigated and focused on numerical simulations, a compact physical, short channel V_{th} model is highly desire to provide efficient guideline for device design.

The most popular V_{th} definition used in compact modeling is the gate voltage at which the bend bending reaches 2 i_B at the silicon surface [8], where Φ_B difference between the Fermi is level and the intrinsic level of silicon in neutral region. Under this condition, the inversion carrier densities at the Si surface equal the density of the dopant atom in the Si bulk NA [8].

The effect of the uniformly doped profile in the Si film can be taken into account by this kind of analysis. In order to analytically model the 2 D characteristics of Double-Gate MOSFET's, the 2 D Poisson's equation must be solved by incorporating suitable boundary conditions. The Green's function technique may give an exact solution for the 2 D Poisson's equation including the uniform doping profile. This advantage was first demonstrated in solving the 2 D potential distribution of a bulk MOSFET by Lin and Wu [3].

In Section-2 the Green's function solution technique for solving the 2 D Poisson's equation in Si regions is introduced and the boundary conditions are also described. The analytic 2 D Threshold voltage in the silicon region is derived exactly and verified by previous 2 D analytical model.

2. MODEL DERIVATION AND VERIFICATION

2.1 The basic analysis

The basic structure of a thin-film DG MOSFET for 2 D analytical model is shown in Fig. 1, the Green's function for a rectangular domain can be expressed in a hyperbolic-sine form, with some Dirichlet and Neumann boundary condition along the rectangular region. The simplified domain for analytically solving the 2 D Poisson's equation and the boundary conditions used are also listed in Table 1. The domain for solving the 2 D Poisson's equation in Si region, as shown in Fig. 1, in which t_{ox} is the front and back gate-oxide region and t_{si} represents the Si film region. Considering the two-dimensional Poisson's equation in a rectangular coordinate system shown in Fig. 1, the 2 D Poisson equation in silicon region is,

$$\Delta^2\Phi(x,y) = -\frac{\rho(x,y)}{\varepsilon_{Si}} = \frac{qN_A f(y)}{\varepsilon_{Si}}, \quad 0 \le y \le t_{Si} \text{ and } 0 \le x \le L$$

Where N_A is substrate doping concentration and $f(y)$ is the doping profile in Si region, Although the 2 D Poisson's equations in the front and back oxide regions are reduced to the 2 D Laplace equations, because charge density is neglected in oxide region.

***Table 1** – The boundary condition relating to the DG MOSFET shown in Fig.* 1

$\Phi(0,y) = V_{bi}(y)$	$0 < y < t_{Si}$
$\Phi(L,y) = V_{bi}(y) + V_{ds}$	$0 < y < t_{Si}$
$D_{Sf}(x,0) = \varepsilon_{Si} E_y(x,0)$	$0 < x < L$
$D_{Sb}(x,t_{Si}) = \varepsilon_{Si} E_y(x,t_{Si})$	$0 < x < L$

Where

$$E_y(x,0) = \frac{\partial\Phi(x,y)}{\partial y} = \frac{C_{ox}}{\varepsilon_{Si}}[V_{gs} - V_{fb} - \Phi_S - \frac{Q_0}{C_{ox}}]$$

$$E_y(x,t_{Si}) = \frac{\partial\Phi(x,y)}{\partial y} = -\frac{C_{ox}}{\varepsilon_{Si}}[V_{gs} - V_{fb} - \Phi_S - \frac{Q_0}{C_{ox}}]$$

The Green's function solution technique is still implemented to solve the 2D potential distribution in Si region with different types of boundary conditions on DG-MOSFET's. The Green's function solution in Si region is used and summarized in Table 2.

Substituting the Green's function solution listed in Table 2, into Green's theorem [5], which is given as

$$\Phi(x,y) = \iint \frac{\rho(x',y')}{\varepsilon} G(x,y,;x',y')dx'dy' + \int G(x,y,;x',y')\frac{\partial\Phi}{\partial n'}ds' -$$
$$-\int \Phi(x',y')\frac{\partial G}{\partial n'}ds' \qquad (1)$$

Where $G(x, y, x', y')$ is the Green's function satisfying $\Delta^2 G = -\delta(x - x')\delta(y - y')$, n' is the outward normal direction on the boundary surface, and neglecting the free carriers.

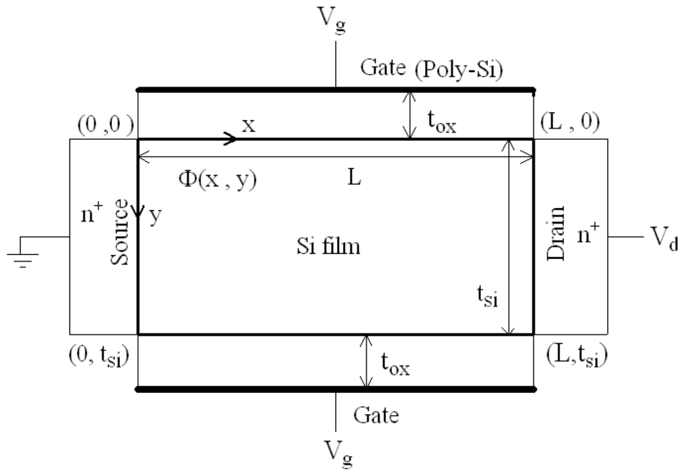

***Fig. 1** – Schematic cross-section of DGMOSFET*

***Table 2** – The solution of Green's function in Si region*

$G_x(x,y,;x',y') = \frac{2}{L}\sum_{n=1}^{\infty}\frac{\sin(k_n x')\sin(k_n x)\sinh(k_n y)\sinh k_n(t_{si}-y')}{k_n \sinh k_n t_{si}}$	$y < y'$
$G_x(x,y,;x',y') = \frac{2}{L}\sum_{n=1}^{\infty}\frac{\sin(k_n x')\sin(k_n x)\sinh(k_n y')\sinh k_n(t_{si}-y)}{k_n \sinh k_n t_{si}}$	$y > y'$
$G_y(x,y,;x',y') = \frac{2}{t_{si}}\sum_{m=1}^{\infty}\frac{\sin(k_m y')\sin(k_m y)\sinh(k_m x)\sinh k_m(L-x')}{k_m \sinh k_m L}$	$x < x'$
$G_y(x,y,;x',y') = \frac{2}{t_{si}}\sum_{m=1}^{\infty}\frac{\sin(k_m y')\sin(k_m y)\sinh(k_m x')\sinh k_m(L-x)}{k_m \sinh k_m L}$	$x > x'$

The equation (1) is general electrostatic potential distribution and it can deal with any arbitrary doping profile in the channel region of Si film where $\rho(x', y') = -qN_A f(y')$ is the charge density of Si region. For simplicity we are assuming Si film as uniformly doped ($f(y') = 1$) in the following analysis. Two dimensional potential equation is obtained

$$\varphi(x,y) = \frac{-qN_A}{2\varepsilon_{si}}x(L-x) + V_{bi} + V_{ds}\frac{x}{L} + \quad (2)$$

$$+\sum_{n=1}^{\infty}\frac{\sin k_n x}{\varepsilon_{si}k_n \sinh k_n t_{si}}[D_{sf}^m \cosh k_n(t_{si}-y) - D_{sb}^m \cosh k_n y] \quad (2)$$

where D_{sf}^m and D_{sb}^m is front and back gate electric displacement. The potential $\Phi(x, y)$ must satisfy the boundary conditions at the SiO_2-Si interface

$$\left.\frac{\partial\Phi(x,y)}{\partial x}\right|_{y=0^+} - \left.\frac{\partial\Phi(x,y)}{\partial x}\right|_{y=0^-} = 0 \tag{3}$$

$$-\varepsilon_{si}\left.\frac{\partial\Phi(x,y)}{\partial y}\right|_{y=0^+} + \varepsilon_{ox}\left.\frac{\partial\Phi(x,y)}{\partial y}\right|_{y=0^-} = 0 \tag{4}$$

After solving equation (3) and (4) and we can obtained

$$D_{sf}^{m} = \frac{\varepsilon_{ox}[B.D\varepsilon_{si}k_n \sinh k_n t_{si} - C\sin k_n x]}{[B.\varepsilon_{si}\sinh k_n t_{si} + B\varepsilon_{ox}\cosh k_n t_{si} - A\varepsilon_{ox}]\sin k_n x} \tag{5}$$

where coefficient

$$A = \frac{\sin k_n x}{k_n}\{\frac{1}{\varepsilon_{ox}} + \frac{1}{\varepsilon_{si}\tanh k_n t_{si}} - \frac{1}{\varepsilon_{si}\sinh k_n t_{si}}\} \tag{6}$$

$$B = \frac{\sin k_n x}{k_n}\{\frac{1}{\varepsilon_{si}\sinh k_n t_{si}} - \frac{1}{\varepsilon_{si}\tanh k_n t_{si}} - \frac{\tanh k_n t_{ox}}{\varepsilon_{ox}}\} \tag{7}$$

$$C = \frac{2\sin k_m t_{ox}}{k_m t_{ox}\sinh k_m L}\{V_{bi}\sinh k_m(L-x) + (V_{bi}+V_{ds})\sinh k_m x\} \tag{8}$$

$$D = \frac{4(V_{gs}-V_{fb})\sin k_n x}{n\pi\cosh k_m t_{ox}} + \frac{qN_A}{2\varepsilon_{si}}x(L-x) - V_{bi} - V_{ds}\frac{x}{L} \tag{9}$$

2.2 Threshold Voltage Model

The position of the minimum surface potential $x_{\min}$ lies on Si surface and can be found by solving

$$\left.\frac{\partial\Phi(x,y)}{\partial x}\right|_{x=x_{\min},y=0,t_{si}} = 0 \tag{10}$$

From Eq. (2), the position of the minimum surface potential $x_{\min}$ can be obtained as

$$\frac{\varepsilon_{ox}\cosh k_n t_{si}}{\varepsilon}\{\frac{qN_A}{\varepsilon_{si}}\frac{x_{\min}(L-x_{\min})k_n}{\tan k_n x_{\min}} - \frac{qN_A}{2\varepsilon_{si}}x_{\min}(L-2x_{\min}) - \frac{V_{ds}}{L} - \frac{2V_{ds}}{L}\frac{x_{\min}k_n}{\tan k_n x_{\min}} - $$
$$- \frac{2V_{bi}k_n}{\tan k_n x_{\min}} + \frac{4(V_{gs}-V_{fb})}{L\cosh k_n t_{ox}\tan k_n x_{\min}}\} - \frac{qN_A}{2\varepsilon_{si}}x_{\min}(L-2x_{\min}) + \frac{V_{ds}}{L} = 0 \tag{11}$$

The position of the minimum surface potential $x_{\min}$ can only be solved by iterative method and no explicit form of $x_{\min}$ can be obtained. The value of $x_{\min}$ by equation (11), the minimum surface potential $\Phi_{sf,\min}$ can be obtained.

$$\Phi_{\min}(x_{\min},0) = -\frac{qN_A}{2\varepsilon_{si}} x_{\min}(L-2x_{\min}) + V_{bi} + V_{ds}\frac{x_{\min}}{L} + \sum_{n=1}^{\infty}\frac{\sin k_n x_{\min}}{\varepsilon_{si}k_n \sinh k_n t_{si}}[D_{sf}^m \cosh k_n t_{si} - D_{sb}^m] = \varphi_{s,\min} \quad (12)$$

The threshold voltage V_{ts} is that value of the gate voltage (V_{gs}) at which a conducting channel is induced at the surface of the DG-MOSFET. The threshold voltage, V_{ts} for the DG-MOSFET model is derived from the analytical approach followed in [13]. The threshold voltage definition in terms of surface potential is taken to be that value of gate source voltage for which $\Phi_{f,inv} = 2\Phi$, where $\Phi_f = V_t \ln(N_A/n_i)$, and $V_{gs} = V_{ts}$. Therefore threshold voltage,

$$V_{th} = V_{fb} + \{2\varphi_f - \frac{qN_A x_{\min}(L-2x_{\min})}{2\varepsilon_{si}} - V_{bi} - V_{ds}\frac{x_{\min}}{L}\}\frac{(\sin k_n x_{\min})^{-1}}{2G_f} - \frac{P}{2G_f} \quad (13)$$

where,

$$G_f = [1-(-1)^n]\frac{R}{d_0}[\frac{2}{m\pi\cosh k_n t_{ox}} + \sum_{m=1}^{\infty}\frac{t}{(m-0.5)\pi}\{(-1)^m - \frac{1}{(m-0.5)\pi}\}]$$

$$R = -\frac{\varepsilon_{si}}{\varepsilon_{ox}}\frac{\tanh k_n t_{ox}}{\sinh k_n t_{si}}$$

$$t = \frac{4}{n\pi}[1 + \frac{L^2(m-0.5)^2}{t_{ox}^2 n^2}]$$

$$d_0 = \frac{1}{(\sinh k_n t_{si})^2} - \{\frac{\varepsilon_{si}\tanh k_n t_{ox}}{\varepsilon_{ox}} + \frac{1}{\tanh k_n t_{si}}\}^2$$

$$T = \sum_{m=1}^{\infty} 2Rt((m-0.5)\pi)^{-2} - \frac{4R}{n\pi}$$

$$P = \frac{1}{d_0}\{[1-(-1)^n]\frac{qN_A L^2}{2\varepsilon_{si}}\frac{8R}{(n\pi)^3} + T[V_{bi}(1-(-1)^n) + V_{ds}(-1)^{n+1}]\}$$

The general short channel V_{th} model is reduced to long channel $\{(L = \infty)$in a long channel threshold voltage model$\}$ one $V_{th,\,long} = V_{fb} - 0.5\mathrm{P}/G_f$. The threshold voltage rolloff ΔV_{th}, which is the difference between short and long-channel V_{th} is obtained,

$$\Delta V_{th} = \{2\Phi_f - \frac{qN_A}{2\varepsilon_{si}} x_{\min}(L - x_{\min}) - V_{bi} - V_{ds}\frac{x_{\min}}{L}\}\frac{(\sin k_n x_{\min})^{-1}}{2G_f}$$

3. RESULT AND DISCUSSION

Fig. 2 and 3 shows the variation of threshold voltage roll-off ΔV_{th} along the channel length for different si film thickness t_{si} = (1.5, 5, 10, and 25 nm) at gate oxide thickness t_{ox} = 1.0 nm and t_{ox} = 1.5 nm at same $V_{ds} = 0.05v$ for proposed analytical model and chen [8].

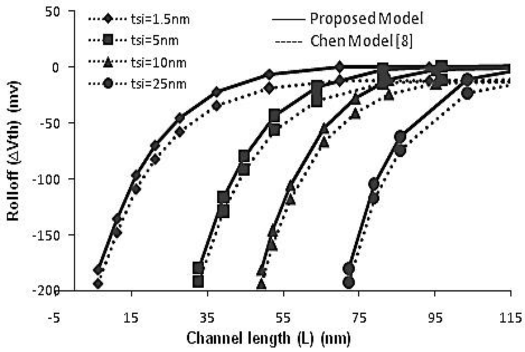

***Fig. 2** – Comparison of the Chen* [8] *and proposed model for the DG-MOSFET,* t_{ox} = 1.0 *nm*

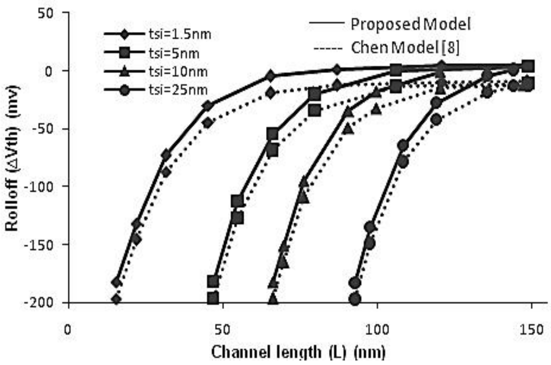

***Fig. 3** – Comparison of the Chen* [8] *and proposed model for the DG-MOSFET,* t_{ox} = 1.5 *nm*

it can be seen from the graph threshold voltage roll-off ΔV_{th} is sensitive to devices parameters like channel length, gate oxide thickness, si film thickness, channel doping concentration and drain bias voltage. It can be seen that as the channel length of the device is decreased, the threshold voltage roll-off increases. The thickness of si film increases, threshold voltage roll-off also increases as it is directly proportional to it. Here gate to gate potential distribution in parabolic type and uniform doping concentration. the curves in this case shifted right side with the increasing silicon film thickness for constant drain to source biasing $V_{ds} = 0.05v$ and constant gate oxide thickness t_{ox} = 1.0 nm and t_{ox} = 1.5 nm the result obtained from our model show the value of threshold voltage roll-off ΔV_{th} is 5-7 % higher than chen model. Fig. 4, we have shown the variation of threshold voltage roll-off along the channel length for different drain bias voltages $V_{ds} = (0.05v, 1.0v)$.

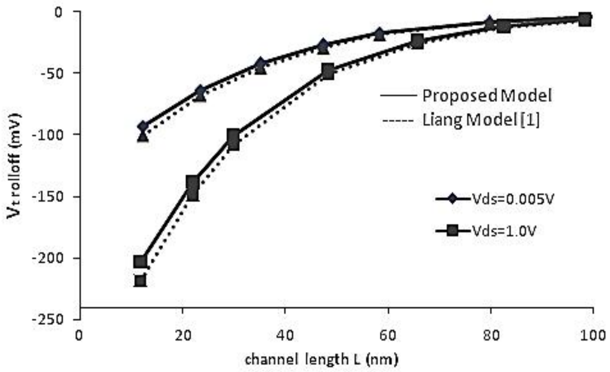

Fig. 4 *– Comparison of the Liang* [1] *and proposed model for the DG-MOSFET.* t_{ox} = 1.0 *nm and* t_{ox} = 1.5 *nm*

The values of other parameters are: gate oxide thickness and t_{ox} = 1.5 nm and silicon film thickness t_{ox} = 1.0 nm. Above figure shows the threshold voltage roll-off ΔV_{th} for both low drain and high drain bias voltages. It can be observed that for higher drain bias, the roll-off is also higher. This is due to the fact that for a fixed high drain bias voltage, the shift in threshold voltage is higher for a long channel device as compared to the short channel device. Our proposed threshold voltage model variation with different parameter in 5-7 % with existed liang [1] model. It has been observed that the proposed model accurately predicts the device behavior and is in well agreement with the existing analytical model such as Liang [1] and Chen [8], with 4-7 % more accurate.

4. CONCLUSION

The exact solution of the 2 D Poisson's equation has been analytically derived by a Green's function solution technique with the suitable boundary conditions in si region. The accuracy of the derived 2 D potential distribution in the si film has been verified by previous analytical model. The above model is valid uniform doping profile in si region. The analytic potential distributions at both front and back surfaces in the si film are same because symmetric DG-MOSFET's. It is shown that the location of the minimum surface potential can only be solved iterative method. Moreover, an analytical threshold voltage model is derived and compared with the previous analytical models. It is clearly shown that good agreement are obtained between the developed threshold voltage model and chen model analysis for wide range of device structure parameter and applied biases. The accurate analytic threshold-voltage model can provide a fast physical analysis of the short-channel effect and further give the scaling rule for deep-submicrometer thin-film so1 MOSFET's in ULSI.

REFERENCES

1. Xiaoping Liang Yuan Taur, *IEEE T. Electron. Dev.* **51,** 1385 (2004).
2. Shih-Ching Lo, Yiming Li, Shao-Ming Yu, *Math. Comput. Model.* **46,** 180 (2007).
3. P.-S. Lin, Ch.-Yu. Wu, *IEEE T. Electron. Dev.* **34,** 1947 (1987).
4. T.K. Chiang, *Semicond. Sci. Tech.* **19,** 1386 (2004).

5. J.D. Jackson, *Classical Electrodynamic* (New York: McGraw-Hill: 1998).
6. Qiang Chen, E.M. Harrell II, J.D. Meindl, *IEEE T. Electron. Dev.* **50,** 1631 (2003).
7. Huaxin Lu, Yuan Taur, *IEEE T. Electron. Dev.* **53,** 1161 (2006).
8. Qiang Chen, E.M. Harrell II, J.D. Meindl, *IEEE T. Electron. Dev.* **50,** 1631 (2003).
9. Hamdy Abd El-Hamid, Jaume Roig, Benjamin Iniguez, *Solid-State Electron.* **51,** 414 (2007).
10. Yawei Jin, Chang Zeng, Lei Ma and Doug Barlage, *Solid-State Electron.* **51,** 347 (2007).
11. R.F. Roach, *Green's Functions: Introductory Theory with Applications* (Van Nostrand Reinhold Company: London: 1970).
12. D. Munteanu, J.L. Autran, S. Harrison, *J. Non-Cryst. Solids* **351,** 1911 (2005).
13. N.D. Arora, *MOSFET Models for VLSI Circuit Simulation – Theory and Practice* (Springer: New York: 1993).